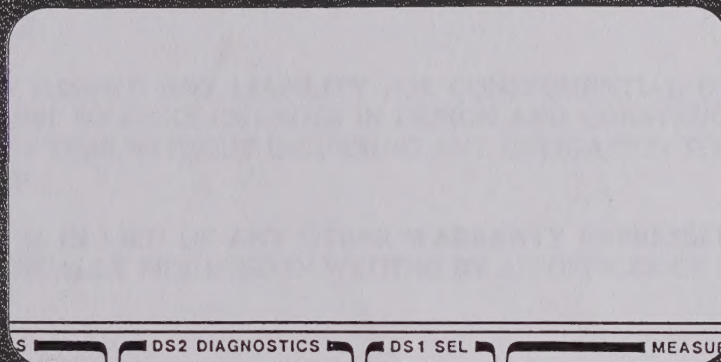


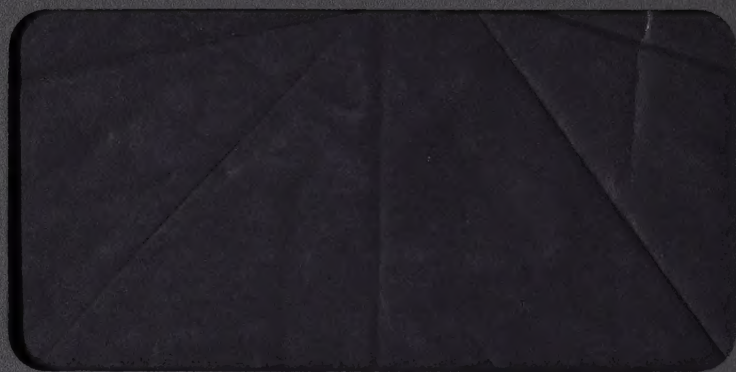
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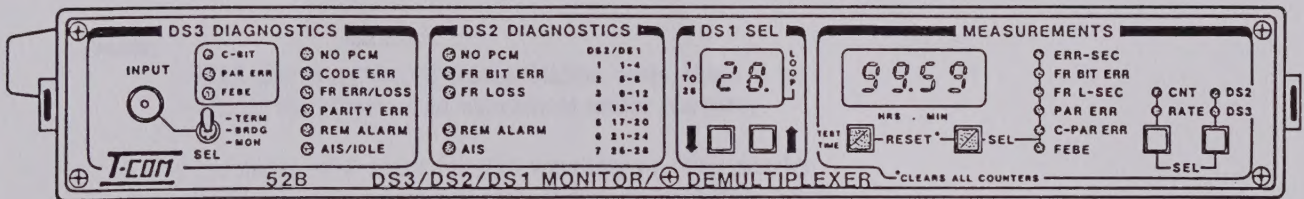


T-COM 52B





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MODEL 52B

INSTRUCTION MANUAL

DS3/DS2/DS1 MONITOR/DEMULPLEXER

Instrument S/N : 52B____

HW/SW Release :

Instruction manual No. : IM052B-001

Date Issued : October 1989

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1. GENERAL INFORMATION

SCOPE

1.1 This instruction and operation manual contains information to install, operate and verify the operational integrity of the T-COM models 52B, 52B-1 and 52B-2 DS3/DS2/DS1 MONITOR/DEMULTIPLEXER.

The small differences between these three versions are clearly identified when appropriate in each section of this manual.

INTRODUCTION

1.2 The model 52B is an add-on module for the T-COM 440B; the 52B-1 is an add-on module for the T-COM 220A/A+ & 320A/A+ series and the 52B-2 is an add-on module for the 440A. Physically, the 52B and 52B-2 differs from the 52B-1 in the fact that only the 52B and 52B-2 are equipped with 3 flat ribbon cables to interconnect it to the 440A/B motherboard. The 52B-1, on the other hand, is not interconnected to the

motherboard of either model. For simplicity, except when the material applies only to the 52B-1 and 52B-2, the text refers to the model 52B in a generic sense.

When combined with a 220A, 320A, 440A or a 440B, the DS3/DS2/DS1 Monitor/Demultiplexer unit provides for the monitoring of the transmission performance at the DS3 and the DS2 rates simultaneously. It also enables the main instrument to access a single DS0 channel from the 672 channels carried by the monitored DS3 bit stream.

The 52B operational features include comprehensive real-time diagnostics at DS3 and DS2 rates along with the capture and the processing of the impairment events. At the same time, the 52B allows the user to select a single DS1 group out of the monitored DS3 bit stream for further analysis by the main instrument or another PCM analyzer.

Generic applications of the 52B include :

- In-service PCM transmission performance monitoring and characterization at DS3 and DS2 rates
- Demultiplexing and accessing a DS1 group for further analysis either at DS1 rate or below

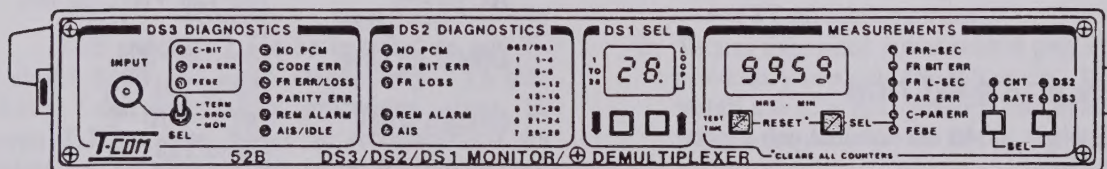


Figure 1.1 Model 52B Front Panel

1.3 PERFORMANCE SPECIFICATIONS

FORMAT COMPATIBILITY

System	DS3 asynchronous (M13 or CBIT Format)
Line	B3ZS (44.7 Mb/s)

DS3 DIAGNOSTICS SECTION

Input jack	75 Ohms, type 440 patch jack
Input modes	TERM (75 Ohms termination) BRDG (635 Ohms bridging)

DS3 DIAGNOSTICS SECTION*(continued)*

	MON (75 Ohms termination/monitor jack)
Input level	Compatible with DSX-3 pulse template as defined in AT&T TA No 34. Also compatible with Hi level ¹
Test display	40 ms per event
Test indicators	
NO PCM	> 250 consecutive 0's
CODE ERR	B3ZS code violation
PARITY ERR	Parity error
FR ERR/LOSS	Error in frame bit time slot (illuminates for 40 ms), Out of frame lock (illuminates for 500ms)
REM ALARM	Selectable X bit state
AIS/IDLE (Red/Green)	AIS Framed 1010...code, selectable w/ or w/o C-bit stuck to 0. IDLE framed 1100...code on CBIT Format.
C BIT	C Bit format
FEBE	Far End Block Error
C PAR ERR	C bit Parity Error
Reframing	Selectable: standard or per Bellcore recommendation TSY-9

DS2 DIAGNOSTICS SECTION

Test display	40 ms nominal per event
Test indicators	
NO PCM	> 250 consecutive 0's
FR BIT ERR	Error in frame bit time slot
FR LOSS	Out of frame lock
REM ALARM	X bit = 0 for over 1 second
AIS	All ones for over 100 microseconds

DS1 SEL SECTION

Group Selection	1 out of 28 with electronic switches
Display type	7 segment LED
Test Indicator	
LOOP	Code as per BellCore recommendation TSY-9

MEASUREMENTS SECTION

Display type	7 segment LED
Display mode	
ERR-SEC	Errored second count
FR BIT ERR	Frame bit error count/rate
FR L-SEC	Frame loss second count
PAR ERR	Parity error count/rate
C-PAR ERR	CBIT parity error count/rate
FEBE/CRC	Far End Block Error/CRC count/rate
TEST TIME	Elapsed time
Counting range	
Counters	0000 to 9999
Rate	9.9 x 10 exp -2 to 0.1 x 10 exp -9
TEST TIME	00.00 to 99.59 (HH.MM)

MISCELLANEOUS

AC power	108-126 VAC, 60 Hz, 12 W
Operating temp	10 to 40 °C (50 to 104 °F)
Storage temp	-30 to +70 °C (22 to 158 °F)
Humidity	Up to 90% non-condensing
Dimensions	2.12" (H) x 13.5" (W) x 10" (D)
Weight	7 lbs (3.2 kg)

ACCESSORIES

IM052B01	Extra instruction manual
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¹ Hi level is the level found at the transmit side output driving the 450 feet of cable leading to the DSX access jacks. For reference, the cable is assumed to introduce a nominal loss of 5 dB at 22.368 MHz.

2. INSTALLATION

INTRODUCTION

2.1 This section contains information and instructions to inspect the new 52B, prepare it for use and to repack it for shipment. Detailed directions for installing the 52B on the model 440B, installing the 52B-2 on the 440A and for installing the 52B-1 on the models 220A/220A+ and 320A/320A+ are also included.

INITIAL INSPECTION

2.2 Inspect the shipping container for damages. Should any damage be found, the container must be kept until all contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify your T-COM representative.

If the shipping container is damaged, notify the carrier as well as the T-COM Representative. Keep the shipping material for the carrier's inspection.

INSTALLATION

2.3 When acquired separately, the 52B and 52B-2 can be installed on any T-COM model 440B and 440A respectively. To this end follow the installation procedure given in paragraph 2.3.1. The 52B-1 is recommended for installation on T-COM models series 220A/A+ and 320A/A+. Follow the steps in the installation procedure given in paragraph 2.3.2 to carry out this installation.

While carrying out either installation procedure, make sure that the instrument is disconnected from the AC line. Refer to figure 2-1.

Installation of the 52B on the model 440B or the 52B-2 on the model 440A

2.3.1 The following procedure refers to the 440B/52B combination but is also applicable to the 440A/52B-2 combination.

1. 440B top cover removal. Remove the 6 screws holding the top cover, using a medium size phillips screwdriver. This top cover is not used with the combination 440B/52B and may be stored away.
2. Remove the 440B rear panel by unscrewing the 6 screws holding it to the rear bezel. To disconnect the cable connecting the power supply to the mother board, firmly grasp the female connector near J21 and lift it from the motherboard. If the 440B is equipped with option 03, remove the cable connecting the DS0 interface board on the rear panel to the mother board at J27.
3. Install the angle bracket A as shown, using a pan head screw 6-32 x 1/4 (B). The threaded hole must be on the vertical member as it is used to retain the 52B rear panel.
4. Install the 52B on top of the 440B instrument, carefully guiding the sides alongside the front and rear bezels.
5. Secure the raised cover with 4 phillips screws previously securing the top cover. In addition, install a 6-32 x 5/16 phillips pan head screw C to secure the raised cover to the angle bracket.
6. Plug the 3 ribbon cables from the 52B to the motherboard male headers labeled respectively J20, J23 (DMUX) and J30 (AUX). Make sure that each connector is properly aligned with its header.
7. Plug the ribbon cable from the rear panel power supply to the mother board male header labeled J21 (PS). If the 440B is equipped with option 03, connect the DS0 interface board on the rear panel to the motherboard male header labeled J27 (DS0).

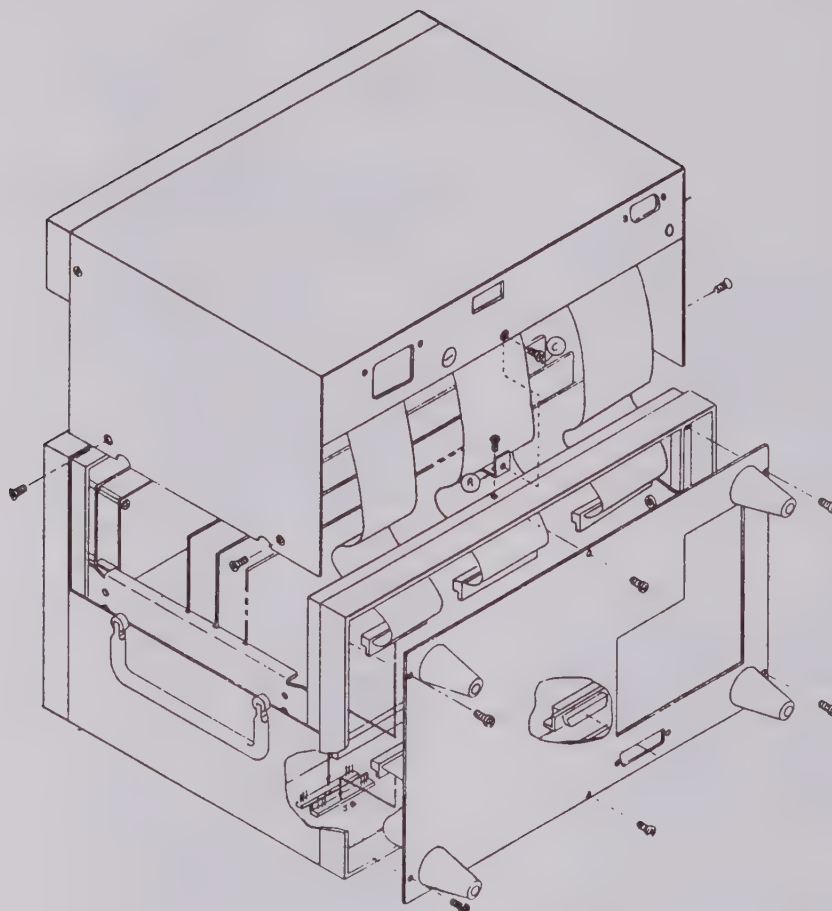


Fig 2-1 52B Installation View on 440B

8. Install the rear panel in place and secure it with the 6 pan head screws previously holding it in place.

This completes the installation procedure for the 52B.

Installation of the 52B-1 on models in the 220A/A+ & 320A/A+ series

2.3.2

1. 220A/320A top cover removal. Remove the 6 screws holding the top cover, using a medium size phillips screwdriver. This top cover is not used with the combination 220A/52B or 320A/52B and may be stored away.

2. Install the angle bracket A as shown, using a pan head screw 6-32 x 1/4 (B). The threaded hole must be on the vertical member as it is used to retain the 52B rear panel.
3. Install the raised cover (52B) on top of the instrument carefully guiding the sides alongside the front and rear bezels.
4. Secure the raised cover with 4 phillips screws previously securing the top cover. In addition, install a 6-32 x 5/16 phillips pan head screw C to secure the raised cover to the angle bracket.

This completes the installation procedure for the 52B-1.

PREPARATION FOR USE

2.4 When the 52B is installed on the 440B according the instructions in paragraph 2.3.1, it is ready for use. The 52B becomes operational when AC power is supplied to both the 440B and the 52B and the 440B power switch is set to ON. Note that this description is also applicable to the 52B-2/440A combination.

When the 52B-1 is installed on the 220A/320A according the instructions in paragraph 2.3.2, it is ready for use. The 52B-1 becomes operational when AC power is supplied to this unit. The powering is independent of the 220A/320A powering and is not controlled by the main instrument power switch.

Note:

To enable the 220A/A+ or 320A/A+ to monitor the selected DS1 group from the 52B-1, the T1 output jack located on the 52B-1 must be patched to Line 1 or Line 2 DS1 input jack. The input selection must be 'TERM' to ensure proper impedance termination.

RACK MOUNTING

2.5 If the combination 52B-2/440A, 52B/440B or 52B-1/220A or 52B-1/320A is to be rack mounted, it is not necessary to use special mounting brackets. The rack mounting brackets available for the 440B/A and the 220A/320A series can be used without modification.

REPACKING FOR SHIPMENT

2.6 All equipment returned to the factory must be accompanied by a T-COM Return Authorization number. In order to get an RA number, customers should call in, or write, with the model and serial numbers of the equipment to be returned **PRIOR TO** shipment. A number will be issued, which will be referenced on both the packing slip and the purchase order associated with the equipment. Include with the instrument a clear description of the encountered problem(s) along with the conditions in which they (it) occur. This can often greatly reduce the cost of repair.

Customer Service Department
T-COM
825 East Middlefield Road
Mountain View, CA 94043
Tel: (415) 964-3415

The use of the original shipping carton and packing material is highly recommended. If the original packing material is not available, any strong container can be used. Wrap the instrument in heavy paper or a plastic bag, and surround it with two or three inches of shock absorbing material to cushion it firmly and prevent movement inside the container.

3. OPERATION

INTRODUCTION

3.1 This section is divided into several important subsections :

- 3.2 and 3.3 explains the functions of the 52B controls and indicators,
- 3.4 describes the operational capabilities of this unit,
- 3.5 provides operating information for this unit when it is used in combination with the 440B and
- 3.6 provides self-testing related information.

Unless specifically noted otherwise, the operation of the 52B-1/220A/320A and the 52B-2/440A is identical to the 52B/440B.

FRONT PANEL FEATURES

3.2 The 52B front panel features are described below. The description numbers match the numbers in figure 3.1.

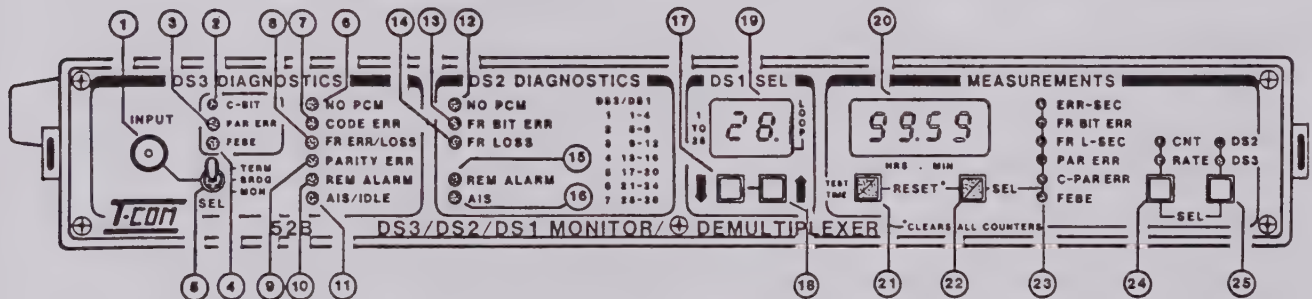


Figure 3.1 Front Panel Features

DS3 Diagnostics section

- 1 **DS3 INPUT** -- This female patch jack accepts only type 440 male plugs. The input circuit is compatible with both Hi and DSX levels regardless of the selection of switch 5.
- 2 **C-BIT** -- This LED is lit when the DS3 signal is in the C Bit Parity format. The format is automatically detected by the 52B.
- 3 **PAR ERR** -- This LED is lit when a C Bit parity error is detected. C Bit parity errors can only occur when the system is in the C Bit parity format. C Bit parity errors are different from parity errors discussed in (9) below.
- 4 **FEBE** -- This LED is lit when a far end block error (FEBE) is detected. These errors can occur only when the system is in the C Bit parity format.
- 5 **SEL** -- This switch configures the input circuit to accept DS3 signals supplied from an unterminated source (TERM), a terminated source (BRDG) or from a monitor access (MON). To operate this switch, the toggle must be pulled toward the user, moved to the desired setting and released. This locking mechanism protects against inadvertent selection changes.
- 6 **NO PCM** -- This LED turns on for 40 ms when the PCM signal presented at the DS3 input consists of a string of 250 or more consecutive zeros. If no PCM signal is presented to the DS3 input (1), this LED is steadily lit.
- 7 **CODE ERROR** -- This LED flashes for 40 ms for each occurrence of a B3ZS code violation. Such a code violation may be 3 or more consecutive zeros or an illegal bipolar violation. If code violations occur at a rate of

25/sec or higher, this indicator may be steadily turned on.

- 8 **FR ERR/LOSS** -- Unless there is FR LOSS, this LED flashes for 40 ms when a frame bit error is detected in the DS3 input signal. Only F bit error occurrences are displayed. When lit for 500 ms, this LED indicates the occurrence of a frame loss. Frame loss occurs when either one or more of the following conditions occur :

- loss of PCM signal for over 250 bits
- 3 frame bits are corrupted in a group of 16 frame bits.
- 3 corrupted M-bit patterns in a row.

Framing recovery criteria depend on rear panel switch selection.

- 9 **PARITY ERR** -- Unless the FR LOSS LED (8) is lit, this LED flashes for 40 ms when a parity error is detected in the DS3 input signal. This LED is lit continuously if the rate of parity error exceeds 25 per second.
- 10 **REM ALARM** -- The lit LED indicates the presence of the remote or yellow alarm as conveyed by the state of the X bit when this condition lasts for over one second while framing prevails. The selection of alarm for X = 1 or 0 is made on the instrument rear panel.
- 11 **AIS/IDLE** -- The red half of this LED is lit when the AIS signal is detected for a minimum of 6 ms. The AIS pattern consists of the framed sequence of 1010.... A rear panel switch provides for selecting compliance with the additional Bellcore requirement for all DS3 C-bits to be set to zero. The green half of this LED is lit when the IDLE signal is detected for a minimum of 6 ms. The IDLE pattern consists of a framed sequence of 1100...

DS2 Diagnostics section

- 12 **NO PCM** -- This LED is lit when the PCM in the selected DS2 group contains a sequence of over 250 consecutive zeros. When the signal is lost, this LED is steadily lit.
- 13 **FR BIT ERR** -- Unless the FR LOSS LED (14) is lit, this LED flashes for 40 ms when a

frame bit error is detected in the monitored DS2 group. Only F bit error occurrences are displayed.

- 14 **FR LOSS** -- When lit, this LED indicates the occurrence of a frame loss. Frame loss occurs when 2 (DS2) frame bits are corrupted in a group of 5 frame bits or when 2 M-bit patterns are corrupted in a row. It should be noted that a loss of PCM for 250 bits does not necessarily cause a frame loss. Framing recovery requires the detection of 8 consecutive uncorrupted frame bits.
- 15 **REM ALARM** -- The lit LED indicates the presence of the remote or yellow alarm when the X bit state is 0 for over one second while framing prevails.
- 16 **AIS** -- This LED is lit when the AIS signal is detected for a minimum of 100 microseconds. The AIS pattern consists of an all ones sequence.

DS1 Selection section

- 17 **DOWN** -- While the reset condition prevails, each brief depression of this switch causes the DS1 group number selection (19) to decrement by one count. If the switch is held depressed for over one second, the selected DS1 group number decrements at the rate of 3 counts per second until it is released.
- 18 **UP** -- While the reset condition prevails, each brief depression of this switch causes the DS1 group number selection (19) to increment by one count. If the switch is held depressed for over one second, the selected DS1 group number increments at the rate of 3 counts per second until it is released.
- 19 **DS1 SEL** -- These two 7-segment LED's display the number of the DS1 group selected as output from the demultiplexer. Any number from 1 through 28 can be displayed. In addition, the decimal point of the least significant digit is lit when the loop code corresponding to the selected channel number is detected. The recognized format is specified by Bellcore in document TSY-9.

Measurement section

- 20 **DISPLAY** -- These four 7-segment LED's display the test time, impairment event counts and bit error rate values in response to the switch selections in the Measurements section. The test time and the event counts are displayed with leading zero suppressed. The test time is displayed in hours and minutes. The bit error rate uses a floating point notation to represent a wider range of values. In this case the display 2.3-7 stands for $2.3 \times 10 \exp -7$.
- 21 **TEST-TIME** -- While this key is depressed, the time elapsed since the last reset is displayed by the four 7-segment display above (20). When this key is depressed at the same time as the SEL key (22), the reset sequence is initiated. More details are given on the reset sequence in section 3.5.1.
- 22 **SEL** -- Like the previous one, this key has a dual function. When depressed by itself, each depression causes the successive selection of data to be displayed as indicated by the LED's (23). When this key is depressed at the same time as the TEST TIME key (21), the reset sequence is initiated.
- 23 **Indicators** -- Except during self-test, only one of these 6 LED's is lit at time. The lit LED indicates the data selection currently displayed.
- 24 **SEL (CNT/RATE)** -- This switch selects whether count or error rate will be displayed. Repeated depressions of this switch toggles the selection between counts and rate. In the count position, errored seconds, frame loss seconds, or counts of errors are displayed. In the rate position, error rates are displayed. When a particular measurement is not applicable to the selected DS2/DS3, or its selected format, the display shows -00-. If the current format is not C Bit, the C bit parity errors or FEBE will not be counted. If the format is changed to C Bit, then the system must be reset (21, 22) to count C Bit parity errors and FEBE's.
- 25 **SEL (DS2/DS3)** -- This key selects the source for the displayed data. Repeated depressions of this key toggles the selection between DS3 and DS2 as indicated by the lit LED's located above the switch. When the DS3 LED is lit, the displayed data is derived from the DS3 Diagnostics section. The displayed data is derived from the DS2 Diagnostics section when the DS2 LED is lit.

REAR PANEL FEATURES

- 3.3 The 52B rear panel features are described below. The description numbers match the numbers in figure 3.2.
- 1 **108-126 VAC** -- This three prong inlet is used to connect the supplied AC power cord to a commercial AC source.
- 2 **1/4 A SB** -- Fuse holder. The required fuse is rated .25 A slow blow.
- 3 **OPERATION CONTROL** -- Only four out of the eight switch positions are active. Their respective assignment is noted on the silkscreened box placed below the switch. Refer to section 3.4.1.1 for additional information.
- 4 **T1 OUTPUT** -- This jack delivers the demultiplexed DS1 group selected by the DS1 SEL section. The bit stream on this jack conforms to the T1 AMI or B8ZS line format. The format is selected by S1-1.
- 5 **CONTROL BIT ACCESS** -- This connection provides for access to the control bit sequence. Refer to section 5.2.5 for additional information.

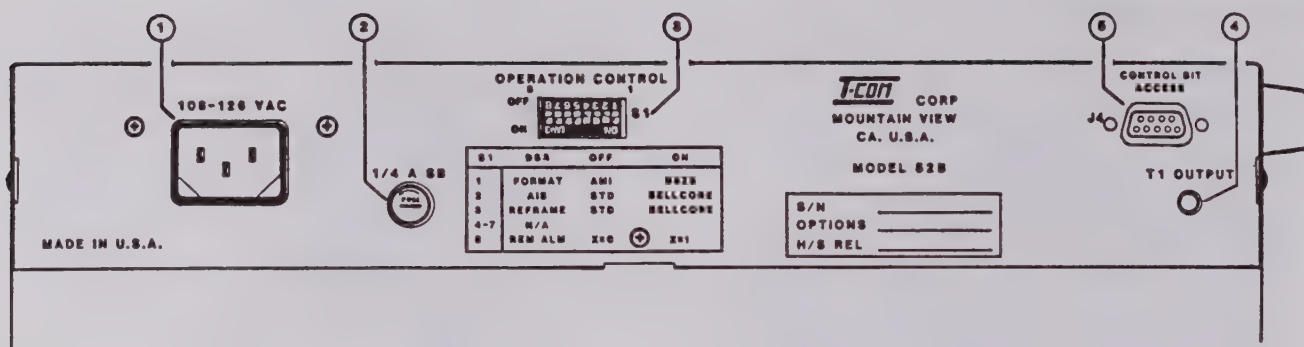


Fig 3.2 52B Rear Panel Features

OPERATIONAL CAPABILITIES

3.4 The 52B offers the following general capabilities :

- DS3 and DS2 real-time transmission impairment diagnostics
- In-service transmission performance characterization, including bit error rate computation
- DS3 to DS1 demultiplexing

These capabilities can be used independently from, or jointly with, the main instrument to which the 52B is secured. They provide an effective way of isolating faults to a particular subsystem or network element. The following sections cover in details the capabilities outlined above.

DS3 and DS2 real-time transmission impairment diagnostics

3.4.1 Real-time transmission impairment diagnostics are provided by the LED's found in the DS3 and the DS2 Diagnostics sections. The DS3 Diagnostics section characterizes the DS3 bit stream presented to the input patch jack. The DS2 Diagnostic section characterizes the DS2 group indirectly selected by the DS1 SEL section.

The DS3 input section is compatible with the level found either at the DSX-3 bay or at the DS3 signal source output (typically an M1-3 multiplexer or a test generator). In this case, the signal is usually referred to as "Hi"; its 22.368 MHz component is approximately 5 dB stronger than at the DSX-3 jack.

Input circuit selection enables the front end to either terminate the line, to provide a high impedance bridge or to comply with the interface requirements of monitor access jacks. (At the monitor jack, the level is attenuated by slightly over 20 dB.)

Warning

When the bridging mode is selected, the 75 Ohm coax cable length from the access point to the 52B DS3 input must not exceed 3 feet. Failure to observe this limitation can cause severe reflections on the monitored circuit resulting in its failure.

Dedicated LED's in the DS3 Diagnostics section display in real-time all impairment occurrences on the DS3 transmission system under observation. All events are stretched to a minimum of 40 ms to ensure visibility. Detailed description of each indicator in this section is provided in paragraph 3.2.

Dedicated LED's in the DS2 Diagnostics section display in real-time all impairment occurrences on the DS2 group selected in the DS3 system under observation. All events are stretched to a minimum of 40 ms to ensure visibility. Detailed description of each indicator in this section is provided in paragraph 3.2.

3.4.1.1 The rear panel mounted dip switch, item 3 in figure 3.2, enables the 52B to be configured so as to conform to various M1-3 multiplexer makes and vintages. The assignments for the various switch positions are given in table 3.1 on the following page.

Sw pos	Settings	Function
1.	ON OFF	B8ZS format for DS1 output AMI format for DS1 output
2.	ON OFF	selects Bellcore recommended DS3 AIS format selects standard DS3 AIS format
3.	ON OFF	selects Bellcore recommended DS3 reframing criteria selects standard DS3 reframing criteria
4 to 7	-	not assigned
8.	ON OFF	DS3 remote alarm is declared when X bit is 1 DS3 remote alarm is declared when X bit is 0

Table 3.1 Rear Panel Switch Assignments

Section 3.5.1 offers some pointers for selecting the appropriate switch settings.

In-service transmission performance characterization

3.4.2 Most of the events displayed by the DS3 or DS2 Diagnostics sections are stored into counters and are processed by a powerful processor to yield directly useable information.

For a given period of observation, the 52B can simultaneously supply all the information found in table 3.2.

Item	DS3	DS2	Description
ERR-SEC	yes	yes	errored second count
FR BIT ERR	yes	yes	frame (F) bit error count & rate
FR LOSS-SEC	yes	yes	frame loss second count
PAR ERR	yes	n/a	parity error count & rate
C-PAR ERR	yes	n/a	C parity error count & rate
FEBE	yes	n/a	Far End Block error count & error rate
TEST TIME	-	-	elapsed test time

Table 3.2 Processed Diagnostics Information

– COUNTS –

Note:

Any counter may be incremented whether its content is being displayed or not.

ERR-SEC -- The DS3 ERR-SEC counter is incremented by one count when, during one second, one or more occurrences of code error and/or parity error and/or DS3 loss of PCM event take place. The

DS2 ERR-SEC counter is incremented by one count when during one second, loss of DS2 PCM occurs.

FR BIT ERR -- This counter is incremented by one count for each detected frame bit error. Counting is disabled while framing is lost. Consequently, if framing is lost for a significant portion of the

FR BIT ERR -- monitored period, the frame bit error count may be lower than fact. Frame bit error counts are further processed to yield the frame bit error rate.

FR LOSS-SEC -- This counter is incremented by one count for each second in which a frame loss condition occurs, whether the frame loss duration lasts a full second or only a fraction of a second. A DS3 frame loss results when 3 frame bits in a group of 16 or fewer are corrupted. A DS2 frame loss results when 2 frame bit errors in a group of 5 or fewer are corrupted.

PAR ERR -- This counter is incremented by one count for each detected parity error. Counting is disabled while framing is lost.

Consequently, if framing is lost for a significant portion of the monitored period, the parity bit error count may be lower than fact. Parity error counts are further processed to yield the parity bit error rate.

C-PAR ERR -- This counter is incremented by one count for each detected C-Bit parity error. Counting is disabled while framing is lost. Consequently, if framing is lost for a significant portion of the monitored period, the C-Bit parity error counts may be lower than fact. The C-Bit parity error counts are further processed to yield the C-Bit parity error rate. Counting is disabled when C-Bit format is not detected or when the incoming format is changed from M13 to C-Bit until a reset is made.

FEBE -- This counter is incremented by one count for each detected far end block error (FEBE). Counting is disabled while framing is lost. Consequently, if framing is lost for a significant portion of the monitored period, the FEBE count may be lower than fact. FEBE counts are further processed to yield the far end block error rate. Counting is disabled when C-Bit format is not detected or when the incoming format is changed from M13 to C-Bit until a reset is made.

– RATES –

The average error rate is obtained by computing, once every three seconds, the ratio of the error count to the total number of observed bits since last reset. To obtain a meaningful error rate reading, all the following conditions must be met :

- a recorded number of errors must be in the range of 4 through 9998
- the test time must be less than 100 hours
- the actual error rate must be greater than $.1 \times 10 \exp^{-9}$
- the patch cord must not be disconnected from the 52B during the period of observation

TEST TIME -- The test time in hours and minutes can be displayed at any time by simply depressing key 21 in figure 3.1. This timer is initialized to __. __0 upon reset.

Non-numeric messages

3.4.2.1 Several non-numeric messages may be displayed in the Measurements section to alert the user to specific conditions. These messages, together with their meanings, are described in table 3.3 below.

Messages	Meanings
8888 flashing	The self test sequence has been successfully completed and the 52B is ready to be reset.
9999 flashing	The counter being displayed has overflowed.
-00-	A non-existent register is called (i.e DS2 PARITY ERR).
99.59 flashing	The test time has exceeded 99:59 hours.

LO E	When displaying the various error rates, this message indicates that either the error count is insufficient (less than 4) or that the error rate is less than $.1 \times 10 \exp-9$.
ILLE	When displaying the error rates, this message indicates that either the error counter has overflowed or the test time has exceeded 100 hours.
Messages	Meanings
CALL	This message indicates that an impairment event has occurred or a count has reached 9999, and no keys have been depressed for the last 90 seconds. Only impairment events that are counted will cause this message to be displayed. This message is removed by depressing any key.

Table 3.3 Non-numeric Messages And Their Meanings

FBER vs PBER for DS3 measurements

3.4.2.2 In actual use, one may observe that the readings obtained for FBER and PBER are not always identical and this could easily lead to confusion. The reading of the next paragraphs discussing the two measurement techniques may help cast some light on this matter.

The FBER gives a highly reliable measure of the actual bit error rate for the overall transmission when the error distribution is uniform. Fortunately, this is the most prevalent case in PCM transmission systems. The FBER measurement is quite precise because it rests on the highly accurate frame bit error count. One should keep in mind that frame bit errors are declared only when a frame bit is detected as having a state opposite to the expected one. One must also note that when monitoring PCM signals exhibiting a low bit error rate, ($1 \times 10 \exp-9$ or less) it takes a relatively long time to acquire a statistically meaningful number of frame bit errors.

The PBER measurement rests on the parity bit error count. It can be shown that the accuracy of this measurement depends on the error rate itself. At low error rate, down to about $10 \exp-7$ the measurement closely tracks the actual bit error rate. When the error rate falls below $10 \exp-7$, the accuracy deteriorates because the parity error count is no longer accurate. This can be readily understood by observing that a parity error is declared only when an odd number of bit errors corrupt a group of 4704 bits (information bits in a DS3 superframe). In turn, this means that at low error rates a single error occurs from time to time and it is picked-up accurately as a parity error. As the error rate grows worse however, the likelihood increases that two bit errors corrupt a

single 4704 bit bundle. Yet because this is an even number of errors, the parity bit count is not affected and the measured bit error rate will thus be somewhat more optimistic than the actual one. As the error rate increases further the accuracy worsens because more than 2 bit errors can corrupt a superframe and only one or no parity bit error is declared.

In a way, it is most fortunate that these two measurements can be performed simultaneously by the test set as they complement each other very well. The FBER is always perfectly accurate but requires longer and longer time as the bit error rate grows smaller. Conversely, the PBER is obtained in a very short time but its accuracy is only dependable when the bit error rate is relatively low. Consequently, if the measurement is to be performed in the shortest time possible, the FBER yields satisfactory accuracy when the bit error rate is $10 \exp-7$ or better; the FBER on the other hand gives high accuracy and requires less and less time as the bit error rate worsens from $10 \exp-7$.

Graphs showing the relationship between PBER and FBER versus actual error rate as a function of the observation time will be provided with the next issue of this manual.

It may be useful to point out that although both FBER and PBER methods have some limitations, the combination can yield an excellent measure of the actual PCM transmission system performance without disrupting the traffic. This is very important when considering that a single DS3 bit streams can simultaneously carry up to 672 calls.

- DS3 to DS1 demultiplexing

3.4.3 The monitored DS3 bit stream can be selectively demultiplexed to yield one of the 7 DS2 groups. At the same time, this DS2 group can be selectively demultiplexed to yield one of the 4 DS1 groups. The organization of the DS2 and DS1 groups follows the hierarchy specified for M1-3 multiplexers. The correspondence between DS1 and DS2 group selection is summarized in table 3.4 on the following page. This table is also silkscreened on the 52B front panel.

DS1	DS2
1 - 4	1
5 - 8	2
9 - 12	3
13 - 16	4
17 - 20	5
21 - 24	6
25 - 28	7

Table 3.4 DS1/DS2 group correspondence

The demultiplexed DS2 group content is analyzed by the DS2 Diagnostics section to yield the real time display of transmission impairment events. As described in previous paragraphs, these events are stored as counts and processed to characterize the transmission performance of this DS2 group.

The demultiplexed DS1 group is not internally characterized by the 52B. Instead, this signal is supplied as a T1 formatted PCM output on the rear panel of the 52B. Refer to jack (4) on figure 3.2. The demultiplexed signal can be analyzed by any T1 compatible PCM test set.

OPERATING INFORMATION

3.5 This section provides information intended to facilitate the use the 52B for its intended purposes.

This section covers :

- Preparation for operation
- Operating modes description

Preparation for operation

3.5.1 Rear panel switch selection

The switches on the 52B rear panel, described in table 3.1, should be set according to the DS3 facility transmission format. This is necessary to ensure consistency of the 52B DS3 diagnostics with the problems observed by the equipment under test. Some pointers for selecting the appropriate switch settings are given below.

Position 1

This position is used for selecting either AMI or B8ZS in the T1 output signal. It is usually set to OFF (AMI) unless otherwise required.

Positions 2 and 3

If the equipment under test conforms to the Bellcore recommendations TSY-9, this switch should be set to ON. Otherwise, select the OFF setting.

Positions 4 to 7

These positions are not assigned and thus the selection is indifferent.

Position 8

In most DS3 equipments, the remote alarm is transmitted by setting the X bit to state 0. Consequently the selection for this switch should be OFF unless otherwise required.

Powering

Powering of the 52B requires a separate power cable to the AC line. In the 52B and 52B-2, power is controlled by the companion 440B or 440A power switch. In the 52B-1 on the other hand, no such linkage exists with the companion instrument and power is applied upon connecting the AC power cord from the 52B-1 to the AC power line.

Interconnection

When the demultiplexed output of the 52B-1 is to be analyzed by the 220A/A+ or 320A/A+, the T1 output from the 52B-1 must be patched to either DS1 line input and the DS1 input selection must be set to TERM. Because the 52B and 52B-2 supply a copy of the T1 PCM output to the 440B and 440A line 1 input via the internal ribbon cables, this external patching is unnecessary. In this case however, this connection prevails only as long as no plug is inserted into the DS1 line input jack.

Self-test

Upon power-up, the 52B executes a comprehensive self-test routine to ensure accuracy of the event counting capability. If the self-test reveals no irregularity, the Measurement section display flashes '8888' at a rate of one flash per second indicating its readiness to start normal operation.

Self-test failure

If a problem is discovered during the self-test, a specific diagnostic message is displayed and further event counting is prevented. However, this failure in the 52B may be temporarily passed over by pushing the test time button. A list of possible failures and their codes are given in Table 3.5. Note, that although the equipment will continue to operate, the characteristic associated with the failure will not work correctly and the equipment should be returned to T-COM for repair as soon as possible. In the event of a failure, it is recommended to turn the power off and to restore it a moment later as occasionally the encountered problem is of a transient nature and not a permanent failure.

Resetting

When the display flashes '8888', the unit must be manually reset to clear all the counters and initialize the test timer. This is accomplished by briefly depressing at the same time keys 21 and 22 in figure 3.1. When this action takes place, the LED's in each of these two keys turn on for approximately 2.5 seconds and turn off. Upon turning off, a reset pulse is delivered by the 52B or 52B-2 (but not by the 52B-1) to the 440A or 440B to clear all the counters. Once cleared, all impairment event counters are ready to accept event counts.

DS3 Input selection

As soon as the instrument is operational, the DS3 input may be patched to the transmission to be monitored and/or demultiplexed. To ensure meaningful analysis, it is essential that the INPUT SEL switch be set as required by the situation. This switch must be set to the TERM position when the input is patched directly to a DS3 signal source output (i.e. M1-3 multiplexer or DS3 signal generator) when no other 75 Ohm termination is provided. In this case, the 52B input provides the proper termination. The BRDG (bridging) setting must be used when the 52B input is patched, in a high impedance manner, onto a transmission system that is normally terminated. The bridging access is most frequently provided by a BNC 'T' connector. The INPUT SEL switch must be set to the MON position

when the input is patched to a monitor jack. Such jacks are typically found at the DSX-3 bay. The input selection is independent of the actual level found at the access point. Once the input selection is properly set, it is only required that the observed signal level be in the range of DSX level to Hi level for the set to accommodate the presented bit stream.

IMPORTANT REMARK

Whereas the cable length of the patch cord is non-critical in both the TERM and the MON mode and can reach upward of 20 feet, it is essential that this cable length does not exceed 3 feet when the BRDG mode is selected. Should a longer patch cord be used in this mode, the 52B no longer presents a high enough impedance to the line to be ignored. Moreover undesirable reflections may be introduced in the observed system by this unterminated cable. These reflections CAN CAUSE MALFUNCTION of the observed system. The user should be cautioned that occasionally, the operation of some systems may be disrupted with cable length shorter than 3 feet.

DS1/DS2 Group selection

The selection of the two demultiplexed groups is controlled by the DS1 SEL section. The two 7-segment LED's in this section display the DS1 group selected. Any DS1 group out of the 28 multiplexed in the DS3 bit stream can be selected by depressing either key below the display. These keys are active upon the resetting of the instrument. For reference, table 3.4 shows the correspondence between DS1 and DS2 group numbers.

Operating modes description

3.5.2 The 52B can be used either by itself or jointly with its companion instrument. It is used independently whenever one requires only DS3/DS2 real-time diagnostic and/or transmission characterization. When it is required to also characterize one of the DS1 groups or to access and analyze the content of one of the 24 channels in a DS1 group, or when it is required to pinpoint a problem in an M1-3 muldem, the use of the combination 52B-2/440A, 52B/440B (or 52B-1/220A+ or 52B-1/320A+) is necessary.

The paragraph below describe the settings required to perform the following tests :

- DS3 real-time monitoring
- DS3 transmission performance characterization
- DS2 real-time monitoring
- DS2 transmission performance characterization
- DS1 real-time monitoring

- DS1 transmission performance characterization
- DS1 channel content characterization
- M13 multiplexing/demultiplexing process characterization

In all cases, the 52B can access the transmission under test by patching the DS3 input jack to any of the jacks shown in figure 3.3.

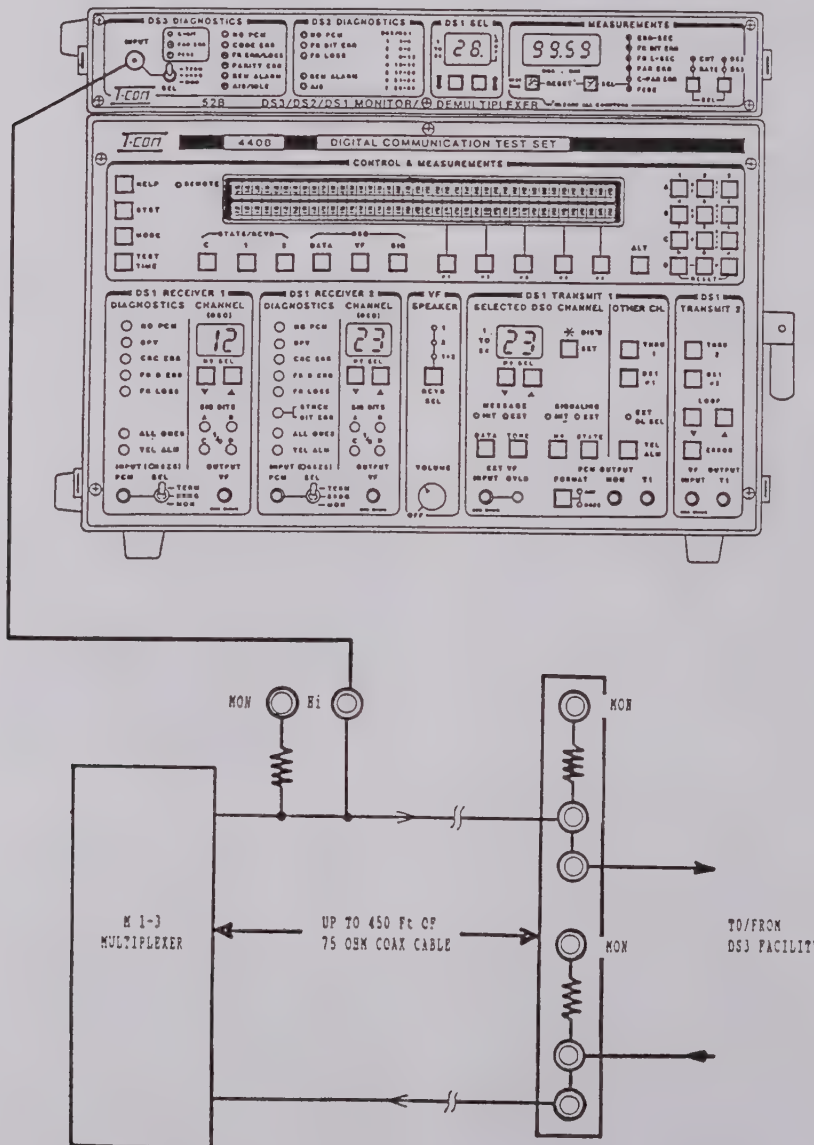


Fig 3.3 52B/440B patching to circuit under test

Real-time DS3 bit stream monitoring

This is immediately possible upon completing the self-testing routine. It requires no additional steps. The states of the LED's in the DS3 Diagnostics section yield the desired information.

DS3 transmission performance analysis

When DS3 transmission performance analysis is required, the 52B Measurements section must be reset and the DS3/DS2 selection should be set to DS3. By repeatedly depressing the SEL key (22) in figure 3.1, one can obtain the reading for each measured parameter over the elapsed test time.

Real-time DS2 group monitoring

The real-time monitoring of a DS2 group in the DS3 bit stream is possible upon completing the self-testing routine. It requires only the selection of the desired DS2 group number. The states of the LED's in the DS2 Diagnostics section yield the desired information.

DS2 transmission performance analysis

When DS2 transmission performance analysis is required, the 52B Measurements section must be reset and the DS3/DS2 selection should be set to DS2. By repeatedly depressing the SEL key (22) in figure 3.1, one can obtain the reading for each measured parameter over the elapsed test time.

Real-time DS1 group monitoring

Real-time monitoring of a DS1 group in the DS3 bit stream starts upon completing the self-testing routine. It requires only the selection of the desired DS1 group number on the 52B and the proper SYSTEM selection on the companion instrument. The states of the LED's in the DS1 Diagnostics section of the 440A, 440B (220A/A+ or 320A/A+ with the 52B-1), yield the desired information.

DS1 transmission performance analysis

When DS1 transmission performance analysis is required, the 52B is configured in the same manner as for performing real-time DS1 monitoring. In addition, the Measurements section source selection on the companion instrument should be set to correspond to the DS1 Diagnostics section receiving the DS1 stream delivered by the 52B. By scanning the DS1 impairment event counters a full characterization of the selected DS1 group can be obtained.

DS1 channel content characterization

The content of a single DS0 channel out of the 672 DS0 channels carried by a DS3 bit stream can be examined and evaluated by letting the companion unit monitor the channel selected out of the demultiplexed DS1 stream delivered by the 52B. Selection of the DS0 channel is obtained with the DS0 channel number selector in the Channel Monitor section. If the channel carries a tone, its level and frequency can be measured directly by the set. The signaling states are simultaneously displayed by bi-color LED's in the Channel Monitor section.

Pinpointing M1-3 muldem problems

Interestingly, by capitalizing on the dual DS1 monitoring capability of the companion unit, it is possible to compare on a real-time basis a DS1 group selected from the DS3 bit stream with the DS1 bit stream originally supplied as an input to the M1-3 multiplexer. Alternatively, the DS1 group selected from the DS3 bit stream can be compared with the DS1 bit stream obtained as an output from a M1-3 demultiplexer. These comparisons can positively characterize the multiplexing and the demultiplexing processes respectively.

To compare the DS1 group obtained from the monitored DS3 bit stream with the corresponding DS1 bit stream supplied as an input to the multiplexer, simply patch to the second DS1 input of the companion instrument a copy of the original DS1 bit stream. The comparison of the two DS1 Diagnostics section LED's as well as the study of the SLIP DSPL (display) can yield valuable information regarding the integrity of the bit stuffing process. When the two bit streams are found to be in full synchronism and exhibit no discrepancies over time in the impairment event counts, the multiplexing process, can be positively exonerated.

To compare the DS1 group obtained from the monitored DS3 bit stream with the corresponding DS1 bit stream delivered by the demultiplexer, simply patch to the second DS1 input of the companion instrument a copy of the DS1 bit stream delivered by the multiplexer.

SELF-TESTING

3.6 As previously noted, the 52B self-testing routine is executed automatically at power-up. This ensures that the user is alerted of any malfunction before the monitoring capability is used.

The self-testing routine performs a comprehensive operational check of all the event counting and processing capabilities.

The self-testing procedure sequentially carried out is outlined below :

- EPROM and internal memory check-out
- individual event latches and counters operation is validated
- all discrete LED's are turned on at the same time for about 4 seconds to provide a lamp-test
- each 7-segment LED displays sequentially the digit 8

- the DS1 line number takes the value 1 and the measurements display takes the value 8888
- the measurement display flashes the value 8888 at the rate of one flash per second until the instrument is manually reset.

If, while carrying out the self-test routine, the microcontroller encounters an operational discrepancy, it flags the problem area by displaying one of the codes listed in table 3.5 below and stop further operation. When the operation stops, no response results upon depressing any key on the 52B front panel except for the test time key (21). See self-test failure, paragraph 3.5.1.

Code	Failed latch or counter	Testing order
EP 0	EPROM checksum error	1
ER 0	RAM error	2
E3 0	DS3 frame loss latch	3
E3 1	DS3 frame bit err counter	4
E3 3	DS3 parity err counter	5
E3 4	DS3 Cbit parity err counter	6
E3 5	DS3 FEBE err counter	7
E3 6	DS3 NO PCM latch	8
E3 7	DS3 REM ALM latch	9
E3 8	DS3 AIS latch	10
E3 9	DS3 CODE ERR latch	11
E3 -	DS3 IDLE latch	12
E2 0	DS2 frame loss latch	13
E2 1	DS2 frame bit err counter	14
E2 6	DS2 NO PCM latch	15
E2 7	DS2 REM ALM latch	16
E2 8	DS2 AIS latch	17
E1 -	DS1 Loop latch	18
ES 0	Serial port loop back error	19

Table 3.5 Self-test Failure Codes Description

These codes are helpful for troubleshooting purpose.

4. TECHNICAL DESCRIPTION

This section is in preparation. It will be released with the next issue of the manual and will be sent to those from whom we have received the warranty registration card.

5. REAR PANEL INTERFACE

INTRODUCTION

5.1 This section contains the information necessary for using the interfaces provided on the 52B rear panel.

DESCRIPTION OF ELECTRICAL INTERFACES

5.2 The rear panel of the 52B contains five items such as connectors and other circuit elements. These are as follows :

- AC Power Input Connector
- Fuse
- (S1) Set of 8 Configuration switches
- T1 Output jack
- Control Bit Access (J4)

AC POWER INPUT CONNECTOR

5.2.1 The 52B operates from a standard 120 VAC, 60 Hz supply. The acceptable range of voltage and frequency are :

Voltage	:	108 to 126 VAC
Frequency	:	58 to 63 Hz

A 6-foot, 3-conductor AC power cord, supplied with the model 52B matches the rear panel AC connector.

PROTECTIVE FUSE

5.2.2 The fuse holder located near the AC power input connector contains a 1/4 amp slow-blow fuse. Failure of the fuse indicates a malfunction. Do not attempt to replace the fuse with one of a higher rating, as this could result in additional damage to the instrument.

CONFIGURATION CONTROL SWITCH

5.2.3 This set of configuration switches is marked S1 on the rear panel and is numbered from right to left. The selection of the four active switches (out of eight) enables the 52B to be configured to comply with specific transmission parameters. Refer to paragraph 3.4.1.1 for details.

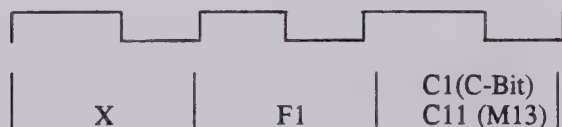
T1 OUTPUT

5.2.4 This bantam jack delivers the PCM bit stream associated with the selected DS1 digroup. The signal is T1 formatted; the peak-to-peak amplitude is 6.0 Volts nominal when terminated into a 100 Ohm resistive load. The signal is delivered to the tip and the ring of the jack and is floating with respect to ground.

CONTROL BIT ACCESS

5.2.5 This connector provides for access to the DS3 control bit sequence. Three signals are provided, (1) a 526 kHz control bit clock, (2) the DS3 control bits and (3) the control bit sync pulse that occurs once every superframe (i.e. 56 control bits). These signals are compatible with 74HC logic.

--> | 1.27us | <--



Control Bit Clock J4-3 (526 kHz)

Control Bits J4-4

Control Sync J4-2 (9398 Hz)

Ground J4-1

6. MAINTENANCE

INTRODUCTION

6.1 This section contains instructions for cleaning and performing the calibration of the model 52B. The cleaning of the instrument can be performed by anyone. To complete the calibration requires a person comfortable with light mechanical assembly/disassembly process and to work with live electrical circuits.

Repair instructions for the set are not provided as these repairs typically require highly specialized test equipment and training. Repairs are most economically performed at the factory.

CLEANING INSTRUCTIONS

6.2 The enclosure exterior surfaces may be cleaned occasionally using a mild soap solution. The use of detergents and mineral spirits must be avoided on the painted surfaces.

CAUTION

To avoid potential hazards introduced by water electrical conduction, the instrument must be disconnected from the AC power line and its power switch must be set to the OFF position during the cleaning process. Let the instrument dry completely before restoring AC power.

CALIBRATION INSTRUCTIONS

6.3 Annual calibration of the 52B is recommended to ensure that all adjustments are optimal. This calibration should not be attempted if the unit fails to satisfactorily complete the self-test routine as this failure cannot result from miscalibration. The calibration consists primarily in adjusting two capacitive trimmers associated with two clock recovery circuits.

Calibration of the 52B requires its separation from the main instrument (440A, 440B, 220A/A+ or

320A/A+) and its disassembly. To separate the 52B from the main instrument, refer to the installation instructions in section 2. These instructions should be carried-out in reverse order.

The disassembly of the 52B consists in freeing the PC board assemblies from the metal enclosure. This is accomplished by following the steps in the next paragraph. The use of a medium size phillips screwdriver is required.

- 52B Disassembly

6.3.1 The bezel is retained to the enclosure by four flat head phillips screws. When these screws are removed, gently pull out the bezel from the assembly.

To access the four phillips screws securing the PC board assemblies to the enclosure, it is convenient to place the top of the 52B flat on the bench. Two screws are located on each side bracket riveted to the inside of each vertical panel. When the four screws are removed, the PC board assemblies can be pulled-out. While handling these assemblies, care must be taken to avoid changing the position of the LED's as this will make the alignment with the front panel more difficult.

When the PC board assemblies are freed from the enclosure, they may be open, as a book, to access the capacitive trimmers. To this end, remove the four phillips screws holding the top and bottom assemblies together. When these screws are removed, separate the two boards as you would open a book, the two boards should be laying flat on the solder side but remain electrically interconnected by the two ribbon cables.

- Preparation for powering

6.3.2 Prior to powering the 52B, it is necessary to bypass the contacts of the power relay normally controlled by the main instrument. To this end an insulated jumper must be soldered, on the solder side, across terminals 7 and 12 of K4 (near the

fuse holder) as shown figure 6.1 below. This jumper has a length of approximately one inch and can be made with AWG #24 or larger plastic insulated

copper wire. The above procedure should be skipped for the version 52B-1 as it does not have a power relay.

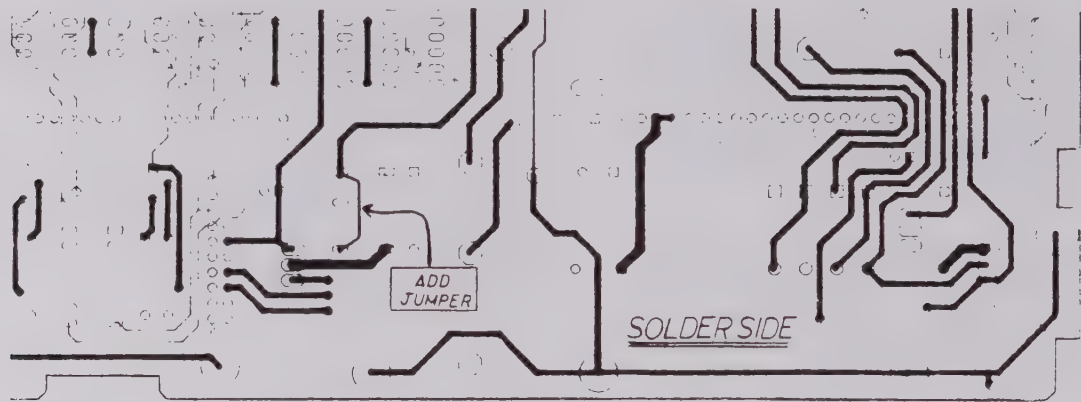


Fig 6.1 Shorting K3 relay contacts

To ensure that no short circuits result when the assembly is under power, the two boards must be resting on an insulated surface. When handling the 52B bottom board assembly, care should be paid to avoid repeated bending of the 3 flat ribbon cables; this precaution will avoid breakage of these cables.

Similarly, it is a sound precaution to minimize wear on the two ribbon cables interconnecting the top and the bottom assemblies. At this point, the assembly is ready to be powered-up.

CAUTION

While AC power is applied to the assembly, 115VAC is present on the area surrounding the large power transformer. Care must be taken to avoid electrical contact with any circuit in this area as dangerous, potentially lethal, shock can result.

Powering is accomplished by connecting an AC power cord between the AC inlet on the lower board assembly and the 115VAC power line.

Generic name	Recommended set
DS3 pattern generator	Tau-tron S5200D transmitter
10 MHz frequency counter	HP 5314A
DVM or DC voltmeter	any
Oscilloscope 100 MHz bw	Phillips PM3267
Low cap 10X probe	Tektronix P6202A

Table 6.1
Required test instruments

- Required test instruments

6.3.3 A list of the test instruments required to perform the calibration is given above in table 6.1. Any instrument with equivalent capabilities can be substituted.

- Power supply operational check

6.3.4 Prior to performing the calibration proper, it is desirable to verify that the power supply voltages and ripple levels are within specifications. Refer to table 6.2 for acceptable range of values applicable to the supply voltages. When testing for level and 60 Hz ripple, the instrument return lead must be grounded. The heat sink on which the AC inlet is secured can be used as ground.

Connector /Pin	Voltage Range	Ripple (mV pk-pk)
P1/4	4.80 to 5.20	50 max (60 Hz)
P1/3	-4.80 to -5.20	50 max (60 Hz)
P1/1	11.50 to 12.50	50 max (60 Hz)

Table 6.2
Power supply requirements

With an oscilloscope connected as listed in table 6.2, verify that the peak to peak ripple is within the tolerance listed for each voltage. Ignore the high frequency noise, only the 60 Hz component is important here.

- DS3 Front-end operational check/calibration

6.3.5 The DS3 front-end calibration requires the patching of one of the six S5200D DS3 outputs directly to the 52B top assembly DS3 input.

- Set the S5200D controls as follows :

Power	: on
Error mode	: Error free
Frame	: DS3-Frame
Pattern	: 1111 [this requires that one of the rear panel switches be set to 1111]
Level	: DSX
- Set the 52B bottom PCB assembly INPUT SEL to TERM and power the assembly.

The calibration of the DS3 clock recovery circuit requires the adjustment of CT1. This air capacitor trimmer is located near the DS3 input jack; its adjustment requires a small size blade screw driver and to follow the next few steps :

- connect the scope probe tip to TP10.
- connect the scope probe ground to the ground TP located near TP3.
- adjust CT1 to obtain the maximum amplitude of the sinewave (approximately 250 mV pk-pk)

Remark

When the clock circuit calibration has been completed, all LED's in the DS3 DIAGNOSTICS section should be turned off and only the FR LOSS LED and the AIS LED in the DS2 DIAGNOSTICS section must be lit. If this is not the case, troubleshooting of the assembly by the factory is called for.

- DS1 Front-end operational check/calibration

6.3.6 The calibration of the DS1 clock recovery circuit requires the adjustment of CT3. In the unlikely event that CT3 cannot be adjusted properly, C48 (located near the small shield on the top board) may have to be selected to place CT3 near the middle of its adjustment range when the clock is properly calibrated.

With the DVM connected at TP7, adjust CT3 to read 2.6 to 2.8 VDC. If the rotor blades of CT3 are engaged from a third to two thirds or the way in, the adjustment is satisfactory. If not, it may be necessary to select a different value for C48. If changing C48, be sure to use a capacitor with an NP0 temperature coefficient.

To determine the appropriate value for C48, proceed as follows :

- connect the counter probe to monitor pin 2 of the IC located at the intersection of labels 5 and F on the edges of the top board
- select the value of C48 that brings the counter to read 1.544 MHz within 5 KHz and, with power off, solder this cap in place.

- Final steps

6.3.7 With CT1 and CT3 adjusted, the calibration is now complete. The PC board assembly should be reinstalled in the enclosure. To carry out the reassembly process, it may be convenient to follow the procedure given in paragraph 6.3.1 in reverse order. Because it is much easier to install the front panel while the bezel is in place, it is recommended to separate the front panel from the bezel prior to reassembly. This is accomplished by removing the four phillips screws securing the front panel to the bezel.

